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INVENTORS: Tinghao Frank Wang

TITLE: METHOD FOR SELECTIVELY ETCHING SILICON AND/OR METAL SILICIDES

ATTORNEYS: Jonathan Blanchard, Ph.D.
BRINKS HOFER GILSON & LIONE
P.O. Box 10395
Chicago, Illinois 60610
(312) 321-4200

METHOD FOR SELECTIVELY ETCHING SILICON AND/OR METAL SILICIDES

FIELD OF THE INVENTION

The present invention relates to the field of semiconductor device manufacturing processes and, in particular, to a tungsten silicide, chromium silicide and/or titanium silicide etch chemistry that is highly selective to poly-silicon and gate oxide structures.

BACKGROUND

One of the challenges facing designers of integrated circuits and other semiconductor devices is the need to continually reduce feature size dimensions so as to be able to improve feature densities on semiconductor (or other) wafers and/or dies. For example, one means by which feature density on a die has been improved is through the use of narrow gate electrodes with a tungsten silicide (WSi_x)/poly-Si stack structure. Such a gate structure provides a good poly/SiO_2 interface, good thermal stability and low contact resistance.

However, forming such a narrow gate structure with a vertical profile and no trenching through the thin gate dielectric that lies beneath the WSi_x/poly-Si stack presents a significant challenge for dry etch processes. That is, the etch should be perfectly anisotropic so as to minimize the critical dimension loss and should exhibit high selectivity to the underlying gate oxide. In many cases, fluorine-based etching gases have been used for WSi_x/poly-Si etching because such chemistries provide a high etch rate for the WSi_x. However, these chemistries present a problem because they tend to exhibit a large amount of side etching and low selectivity to the gate oxide. Chlorine-based etching gases provide reduced side etching and higher selectivity to SiO_2, however, the etch rate of the WSi_x is slower than that for fluorine-based chemistries.

In the past, some reported studies have shown that plasma etch using a Cl_2/O_2 gas mixture, with low concentrations of O_2 (i.e., less than 15% O_2 by volume) have exhibited improved WSi_x etch rate, and such chemistries were found to exhibit high poly-Si/SiO_2 selectivity. However, these same studies reported that as the O_2 concentration increased above approximately 20%, the WSi_x and ploy-Si etch rates were dramatically reduced. Indeed, the studies report that the etching stops when the O_2 concentration exceeds 25%. See, e.g., Kazuo Nojiri et al., "High Rate and Highly Selective Anisotropic Etching for WSix/Poly-Si Using Electron Cyclotron Resonance Plasma," J. Vac. Sci. Technol. B 14(3) May/Jun 1996. Also, the etch was not selective between the WSi_x and the poly-Si.

SUMMARY OF THE INVENTION

In one embodiment, a metal silicide (e.g., WSi_x) layer is etched during fabrication of an integrated circuit in a Cl_2/O_2 environment having an O_2 concentration of greater than or equal to 25% (e.g., 25 - 75%) by volume. This environment may be provided at a pressure of approximately 2 - 40 mili-Torr, in a reactor with a source power of approximately 200 - 2000 (and in one example 400) Watts and a bias power of approximately 35 to 400 (and, in one example 50) Watts for approximately 30 seconds. In one particular example, 9 the Cl_2/O_2 environment includes approximately 45 sccm Cl_2 and 30 sccm O_2.

In a further embodiment, a metal silicide layer is etched during fabrication of an integrated circuit in an environment having a high concentration of O_2 so as to fully etch the WSi_x layer without etching an underlying poly-silicon layer. Preferably, the O_2 concentration is greater than or equal to 25% by volume.

In another embodiment, an integrated circuit includes a metal silicide layer etched within an environment that provides high selectivity to poly-silicon, for example an environment that includes a concentration of O_2 of at least 25% by volume (e.g., 45 sccm Cl_2 and 30 sccm O_2). The metal silicide layer may be a portion of a gate structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not limitation, in the accompanying figure, which illustrates various steps during the fabrication of an integrated circuit (e.g., a gate structure therein) in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

An etch chemistry for tungsten silicide, chromium silicide and/or titanium silicide that is highly selective to poly-silicon and gate oxide structures is disclosed herein. Although discussed with reference to certain illustrated embodiments, upon review of this specification, those of ordinary skill in the art will recognize that the present methods may find application in a variety of systems. For example, much of the following discussion will focus on a WSi_x etch, but it should be recognized that the techniques are equally applicable to a chromium silicide or titanium silicide etch. Therefore, in the following description the illustrated embodiments should be regarded as exemplary only and should not be deemed to be limiting in scope.

Through experiment, it has been determined that a Cl_2/O_2-based etch chemistry wherein the O_2 concentration is greater than or equal to 25% (e.g., 25 - 75 %) by volume provides a WSi_x etch that is highly selective (e.g., a ratio of etch rates on the order of 30 or more) to poly-silicon, silicon, nitride and oxides (e.g., gate oxides). Indeed, oxide and nitride selctivities on the order of 100 or more have been observed. To more fully appreciate the present etch process, one should make reference to the layer structure presented in the accompanying figure.

As shown in the upper illustration of the figure, in creating gate structures a gate oxide layer 15 is grown (e.g., through thermal oxidation) over a substrate 10. Such gate oxide layers may be from 25 - 70Å thick. Next, a poly-Si layer 20 of approximately 1000Å is depositied over the oxide and a WSi_x layer 25 of approximately 1000Å is deposited thereover. On top of the WSi_x layer 25, a nitride mask layer 30 (e.g., approximately 2000Å thick) is deposited and patterned through the use of a conventional photoresist layer 35.

After patterning, the photoresist layer 35 is stripped off (see the second and third illustrations in sequence) and the etch of the WSi_x layer 25 can be commenced. The goal of this etch is to completely remove the WSi_x (except in those areas under the nitride mask) without etching the underlying poly-Si layer 20. As can bee seen from the Nojiri article cited above, previous etch chemistries did not allow for the control of this etch so as to stop on the poly-Si. In other words, these previous etch chemistries were not selective between WSi_x and poly-Si.

The present etch chemistry, however, does provide a high degree of selectivity between WSi_x and poly-Si. As indicated above, a ratio of etch rates in WSi_x and poly-Si of 30:1 or more has been observed. This provides the high degree of selectivity needed to ensure that the etch can be stopped on the poly-Si layer 20 as desired. Afterwards, a conventional poly-Si etch and gate oxide removal process can be used to finish forming the gate structure.

The present WSi_x etch employs a Cl_2/O_2 chemistry, with a high concentration (e.g., greater than or equal to 25%, for example 25 - 75 %, by volume) of O_2. Contrary to the results reported by Nojiri, under the present etch conditions it has been observed that even in such high O_2 concentration, WSi_x is etched. In one example, the etch was performed using a LAM 9400 high density plasma reactor, available from LAM Research of Fremont, CA. Prior to the Cl_2/O_2 etch, a brief (e.g., approximately 5 second) breakthrough etch using CF_4 was performed. Then, the Cl_2/O_2 etch was performed at a pressure of approximately 3 mili-Torr (mT) (or, more generally, a low pressure of approximately 2 - 40 mT), a source power of approximately 400 W (or, more generally, approximately 200 - 2000 W), a bias power of approximately 35 to 400 (e.g., 50) W, in an environment of approximately 45 sccm Cl_2 and 30 sccm O_2 for approximately 30 seconds. Note that in practice the etch time may vary

depending on the film thickness. Under the above conditions, a WSi_x etch rate of approximately 1639 Å/min was observed. The WSi_x layer (approximately 1000Å) was completely etched, while the underlying poly-Si layer was not etched to an observable degree.

The present etch chemistry for WSi_x provides an improved process window (over that provided by schemes of the past) for structures wherein WSi_x overlies a poly-Si layer. For example, the present etch process may be used during the patterning of gate structures or other structures during the fabrication of integrated circuit devices.

Thus a tungsten silicide etch chemistry that is highly selective to poly-silicon and gate oxide structures has been described. Although the foregoing description and accompanying figures discuss and illustrate specific embodiments, it should be appreciated that the present invention is to be measured only in terms of the claims that follow.